



PSoC® Creator™

Project Datasheet for UART_RxTx01

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1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical [CY8C58LP](#) family member PSoC 5 device. For details on all the systems listed above, please refer to the [PSoC 5 Technical Reference Manual](#).

Figure 1. CY8C58LP Device Family Block Diagram

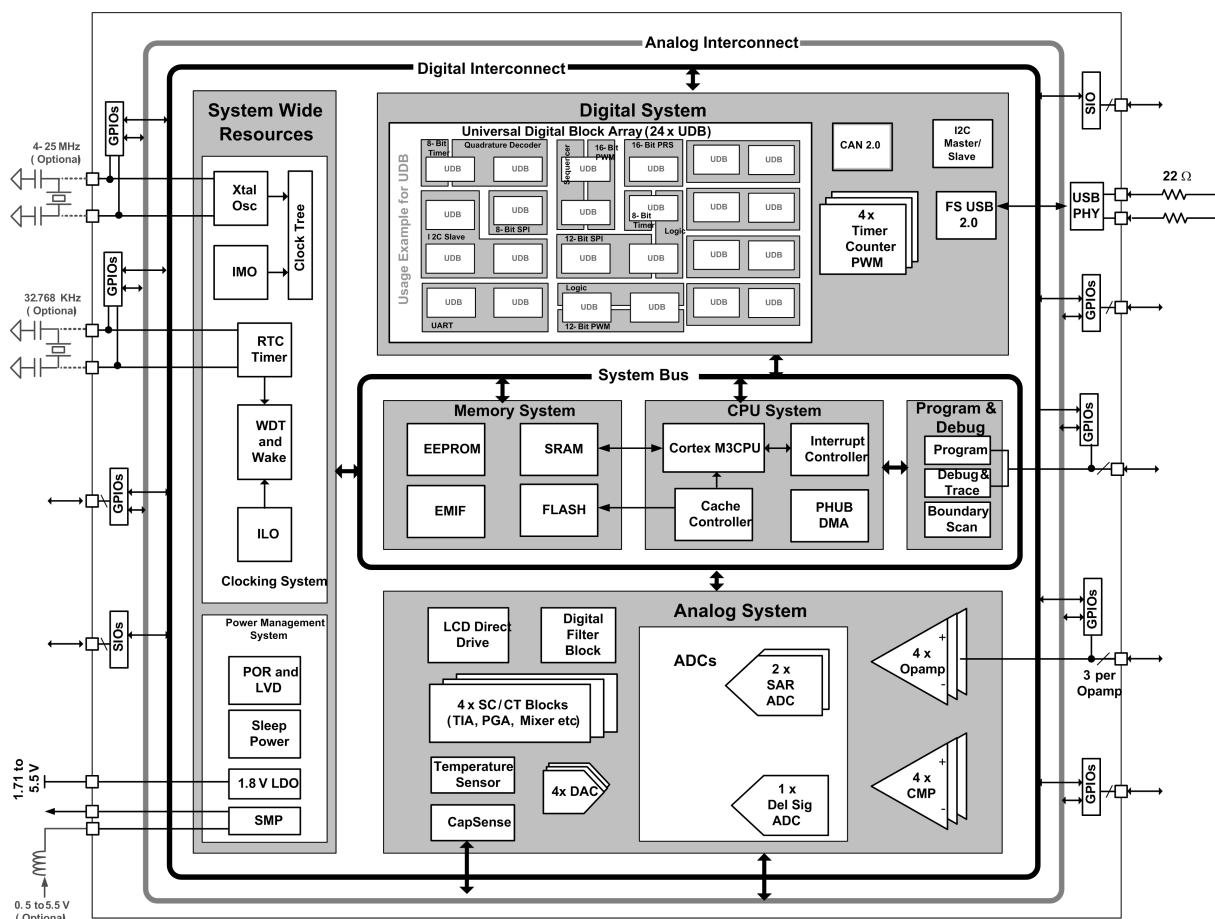


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C5868AXI-LP035
Package Name	100-TQFP
Architecture	PSoC 5
Family	CY8C58LP
CPU speed (MHz)	67
Flash size (kBytes)	256
SRAM size (kBytes)	64
EEPROM size (Bytes)	2048
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85
JTAG ID	0x2E123069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the [System Clocks](#) section below.

Table 2 lists the device resources that this design uses:

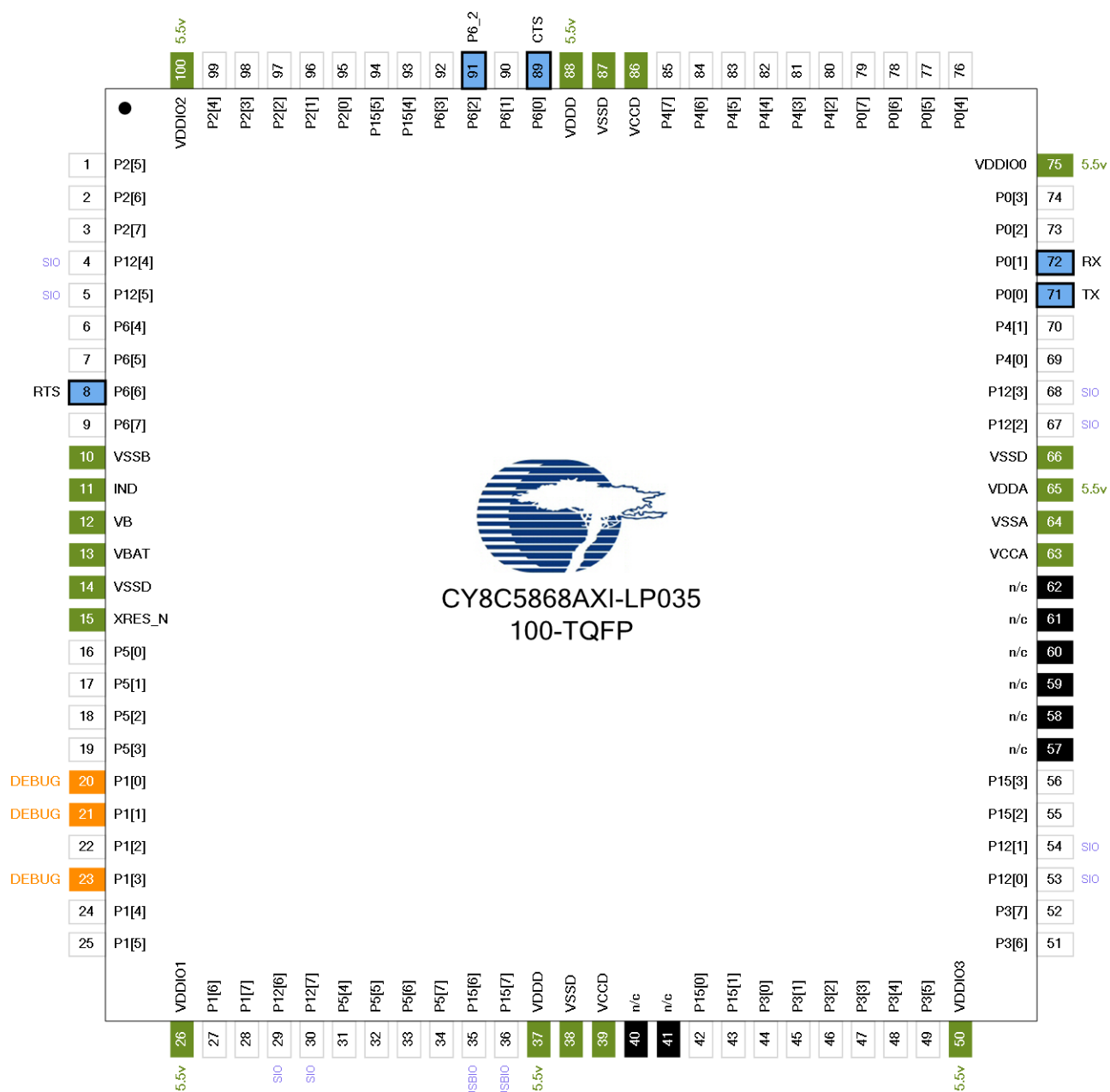
Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Digital Clocks	1	7	8	12.50 %
Analog Clocks	0	4	4	0.00 %
CapSense Buffers	0	2	2	0.00 %
Digital Filter Block	0	1	1	0.00 %
Interrupts	0	32	32	0.00 %
IO	8	64	72	11.11 %
Segment LCD	0	1	1	0.00 %
CAN 2.0b	0	1	1	0.00 %
I2C	0	1	1	0.00 %
USB	0	1	1	0.00 %
DMA Channels	0	24	24	0.00 %
Timer	0	4	4	0.00 %
UDB				
Macrocells	32	160	192	16.67 %
Unique P-terms	54	330	384	14.06 %
Total P-terms	66			
Datapath Cells	3	21	24	12.50 %
Status Cells	5	19	24	20.83 %
StatusI Registers	3			
Routed Count7 Load/Enable	2			
Control Cells	3	21	24	12.50 %
Control Registers	1			
Count7 Cells	2			
Opamp	0	4	4	0.00 %
Comparator	0	4	4	0.00 %
Delta-Sigma ADC	0	1	1	0.00 %
LPF	0	2	2	0.00 %
SAR ADC	0	2	2	0.00 %
Analog (SC/CT) Blocks	0	4	4	0.00 %
DAC				

Resource Type	Used	Free	Max	% Used
VIDAC	0	4	4	0.00 %

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[5]	GPIO [unused]			HiZ Analog Unb
2	P2[6]	GPIO [unused]			HiZ Analog Unb
3	P2[7]	GPIO [unused]			HiZ Analog Unb
4	P12[4]	SIO [unused]			HiZ Analog Unb
5	P12[5]	SIO [unused]			HiZ Analog Unb
6	P6[4]	GPIO [unused]			HiZ Analog Unb
7	P6[5]	GPIO [unused]			HiZ Analog Unb
8	P6[6]	RTS	Dgtl Out	Strong drive	HiZ Analog Unb
9	P6[7]	GPIO [unused]			HiZ Analog Unb
10	VSSB	VSSB	Dedicated		
11	IND	IND	Dedicated		
12	VB	VB	Dedicated		
13	VBAT	VBAT	Dedicated		
14	VSSD	VSSD	Power		
15	XRES_N	XRES_N	Dedicated		
16	P5[0]	GPIO [unused]			HiZ Analog Unb
17	P5[1]	GPIO [unused]			HiZ Analog Unb
18	P5[2]	GPIO [unused]			HiZ Analog Unb
19	P5[3]	GPIO [unused]			HiZ Analog Unb
20	P1[0]	Debug:SWD_IO	Reserved		
21	P1[1]	Debug:SWD_CK	Reserved		
22	P1[2]	GPIO [unused]			HiZ Analog Unb
23	P1[3]	Debug:SWV	Reserved		
24	P1[4]	GPIO [unused]			HiZ Analog Unb
25	P1[5]	GPIO [unused]			HiZ Analog Unb
26	VDDIO1	VDDIO1	Power		
27	P1[6]	GPIO [unused]			HiZ Analog Unb
28	P1[7]	GPIO [unused]			HiZ Analog Unb
29	P12[6]	SIO [unused]			HiZ Analog Unb
30	P12[7]	SIO [unused]			HiZ Analog Unb
31	P5[4]	GPIO [unused]			HiZ Analog Unb
32	P5[5]	GPIO [unused]			HiZ Analog Unb
33	P5[6]	GPIO [unused]			HiZ Analog Unb
34	P5[7]	GPIO [unused]			HiZ Analog Unb
35	P15[6]	USB IO [unused]			HiZ Analog Unb
36	P15[7]	USB IO [unused]			HiZ Analog Unb
37	VDDD	VDDD	Power		
38	VSSD	VSSD	Power		
39	VCCD	VCCD	Power		
42	P15[0]	GPIO [unused]			HiZ Analog Unb
43	P15[1]	GPIO [unused]			HiZ Analog Unb
44	P3[0]	GPIO [unused]			HiZ Analog Unb
45	P3[1]	GPIO [unused]			HiZ Analog Unb
46	P3[2]	GPIO [unused]			HiZ Analog Unb
47	P3[3]	GPIO [unused]			HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
48	P3[4]	GPIO [unused]			HiZ Analog Unb
49	P3[5]	GPIO [unused]			HiZ Analog Unb
50	VDDIO3	VDDIO3	Power		
51	P3[6]	GPIO [unused]			HiZ Analog Unb
52	P3[7]	GPIO [unused]			HiZ Analog Unb
53	P12[0]	SIO [unused]			HiZ Analog Unb
54	P12[1]	SIO [unused]			HiZ Analog Unb
55	P15[2]	GPIO [unused]			HiZ Analog Unb
56	P15[3]	GPIO [unused]			HiZ Analog Unb
63	VCCA	VCCA	Power		
64	VSSA	VSSA	Power		
65	VDDA	VDDA	Power		
66	VSSD	VSSD	Power		
67	P12[2]	SIO [unused]			HiZ Analog Unb
68	P12[3]	SIO [unused]			HiZ Analog Unb
69	P4[0]	GPIO [unused]			HiZ Analog Unb
70	P4[1]	GPIO [unused]			HiZ Analog Unb
71	P0[0]	TX	Dgtl Out	Strong drive	HiZ Analog Unb
72	P0[1]	RX	Dgtl In	HiZ digital	HiZ Analog Unb
73	P0[2]	GPIO [unused]			HiZ Analog Unb
74	P0[3]	GPIO [unused]			HiZ Analog Unb
75	VDDIO0	VDDIO0	Power		
76	P0[4]	GPIO [unused]			HiZ Analog Unb
77	P0[5]	GPIO [unused]			HiZ Analog Unb
78	P0[6]	GPIO [unused]			HiZ Analog Unb
79	P0[7]	GPIO [unused]			HiZ Analog Unb
80	P4[2]	GPIO [unused]			HiZ Analog Unb
81	P4[3]	GPIO [unused]			HiZ Analog Unb
82	P4[4]	GPIO [unused]			HiZ Analog Unb
83	P4[5]	GPIO [unused]			HiZ Analog Unb
84	P4[6]	GPIO [unused]			HiZ Analog Unb
85	P4[7]	GPIO [unused]			HiZ Analog Unb
86	VCCD	VCCD	Power		
87	VSSD	VSSD	Power		
88	VDDD	VDDD	Power		
89	P6[0]	CTS	Dgtl In	HiZ digital	HiZ Analog Unb
90	P6[1]	GPIO [unused]			HiZ Analog Unb
91	P6[2]	P6_2	Dgtl Out	Strong drive	HiZ Analog Unb
92	P6[3]	GPIO [unused]			HiZ Analog Unb
93	P15[4]	GPIO [unused]			HiZ Analog Unb
94	P15[5]	GPIO [unused]			HiZ Analog Unb
95	P2[0]	GPIO [unused]			HiZ Analog Unb
96	P2[1]	GPIO [unused]			HiZ Analog Unb
97	P2[2]	GPIO [unused]			HiZ Analog Unb
98	P2[3]	GPIO [unused]			HiZ Analog Unb
99	P2[4]	GPIO [unused]			HiZ Analog Unb
100	VDDIO2	VDDIO2	Power		

Abbreviations used in Table 3 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- HiZ digital = High impedance digital

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	71	TX	Dgtl Out	Strong drive	HiZ Analog Unb
P0[1]	72	RX	Dgtl In	HiZ digital	HiZ Analog Unb
P0[2]	73	GPIO [unused]			HiZ Analog Unb
P0[3]	74	GPIO [unused]			HiZ Analog Unb
P0[4]	76	GPIO [unused]			HiZ Analog Unb
P0[5]	77	GPIO [unused]			HiZ Analog Unb
P0[6]	78	GPIO [unused]			HiZ Analog Unb
P0[7]	79	GPIO [unused]			HiZ Analog Unb
P1[0]	20	Debug:SWD_IO	Reserved		
P1[1]	21	Debug:SWD_CK	Reserved		
P1[2]	22	GPIO [unused]			HiZ Analog Unb
P1[3]	23	Debug:SWV	Reserved		
P1[4]	24	GPIO [unused]			HiZ Analog Unb
P1[5]	25	GPIO [unused]			HiZ Analog Unb
P1[6]	27	GPIO [unused]			HiZ Analog Unb
P1[7]	28	GPIO [unused]			HiZ Analog Unb
P12[0]	53	SIO [unused]			HiZ Analog Unb
P12[1]	54	SIO [unused]			HiZ Analog Unb
P12[2]	67	SIO [unused]			HiZ Analog Unb
P12[3]	68	SIO [unused]			HiZ Analog Unb
P12[4]	4	SIO [unused]			HiZ Analog Unb
P12[5]	5	SIO [unused]			HiZ Analog Unb
P12[6]	29	SIO [unused]			HiZ Analog Unb
P12[7]	30	SIO [unused]			HiZ Analog Unb
P15[0]	42	GPIO [unused]			HiZ Analog Unb
P15[1]	43	GPIO [unused]			HiZ Analog Unb
P15[2]	55	GPIO [unused]			HiZ Analog Unb
P15[3]	56	GPIO [unused]			HiZ Analog Unb
P15[4]	93	GPIO [unused]			HiZ Analog Unb
P15[5]	94	GPIO [unused]			HiZ Analog Unb
P15[6]	35	USB IO [unused]			HiZ Analog Unb
P15[7]	36	USB IO [unused]			HiZ Analog Unb
P2[0]	95	GPIO [unused]			HiZ Analog Unb
P2[1]	96	GPIO [unused]			HiZ Analog Unb
P2[2]	97	GPIO [unused]			HiZ Analog Unb
P2[3]	98	GPIO [unused]			HiZ Analog Unb
P2[4]	99	GPIO [unused]			HiZ Analog Unb
P2[5]	1	GPIO [unused]			HiZ Analog Unb
P2[6]	2	GPIO [unused]			HiZ Analog Unb
P2[7]	3	GPIO [unused]			HiZ Analog Unb
P3[0]	44	GPIO [unused]			HiZ Analog Unb
P3[1]	45	GPIO [unused]			HiZ Analog Unb
P3[2]	46	GPIO [unused]			HiZ Analog Unb
P3[3]	47	GPIO [unused]			HiZ Analog Unb
P3[4]	48	GPIO [unused]			HiZ Analog Unb

Port	Pin	Name	Type	Drive Mode	Reset State
P3[5]	49	GPIO [unused]			HiZ Analog Unb
P3[6]	51	GPIO [unused]			HiZ Analog Unb
P3[7]	52	GPIO [unused]			HiZ Analog Unb
P4[0]	69	GPIO [unused]			HiZ Analog Unb
P4[1]	70	GPIO [unused]			HiZ Analog Unb
P4[2]	80	GPIO [unused]			HiZ Analog Unb
P4[3]	81	GPIO [unused]			HiZ Analog Unb
P4[4]	82	GPIO [unused]			HiZ Analog Unb
P4[5]	83	GPIO [unused]			HiZ Analog Unb
P4[6]	84	GPIO [unused]			HiZ Analog Unb
P4[7]	85	GPIO [unused]			HiZ Analog Unb
P5[0]	16	GPIO [unused]			HiZ Analog Unb
P5[1]	17	GPIO [unused]			HiZ Analog Unb
P5[2]	18	GPIO [unused]			HiZ Analog Unb
P5[3]	19	GPIO [unused]			HiZ Analog Unb
P5[4]	31	GPIO [unused]			HiZ Analog Unb
P5[5]	32	GPIO [unused]			HiZ Analog Unb
P5[6]	33	GPIO [unused]			HiZ Analog Unb
P5[7]	34	GPIO [unused]			HiZ Analog Unb
P6[0]	89	CTS	Dgtl In	HiZ digital	HiZ Analog Unb
P6[1]	90	GPIO [unused]			HiZ Analog Unb
P6[2]	91	P6_2	Dgtl Out	Strong drive	HiZ Analog Unb
P6[3]	92	GPIO [unused]			HiZ Analog Unb
P6[4]	6	GPIO [unused]			HiZ Analog Unb
P6[5]	7	GPIO [unused]			HiZ Analog Unb
P6[6]	8	RTS	Dgtl Out	Strong drive	HiZ Analog Unb
P6[7]	9	GPIO [unused]			HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- Dgtl Out = Digital Output
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- HiZ digital = High impedance digital

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
CTS	P6[0]	Dgtl In	HiZ Analog Unb
Debug:SWD_CK	P1[1]	Reserved	
Debug:SWD_IO	P1[0]	Reserved	
Debug:SWV	P1[3]	Reserved	
GPIO [unused]	P3[4]		HiZ Analog Unb
GPIO [unused]	P3[2]		HiZ Analog Unb
GPIO [unused]	P15[1]		HiZ Analog Unb
GPIO [unused]	P3[0]		HiZ Analog Unb
GPIO [unused]	P3[1]		HiZ Analog Unb
GPIO [unused]	P3[7]		HiZ Analog Unb
GPIO [unused]	P3[6]		HiZ Analog Unb
GPIO [unused]	P3[5]		HiZ Analog Unb
GPIO [unused]	P3[3]		HiZ Analog Unb
GPIO [unused]	P15[3]		HiZ Analog Unb
GPIO [unused]	P15[2]		HiZ Analog Unb
GPIO [unused]	P0[7]		HiZ Analog Unb
GPIO [unused]	P4[1]		HiZ Analog Unb
GPIO [unused]	P4[0]		HiZ Analog Unb
GPIO [unused]	P0[6]		HiZ Analog Unb
GPIO [unused]	P0[5]		HiZ Analog Unb
GPIO [unused]	P0[3]		HiZ Analog Unb
GPIO [unused]	P0[2]		HiZ Analog Unb
GPIO [unused]	P4[6]		HiZ Analog Unb
GPIO [unused]	P4[7]		HiZ Analog Unb
GPIO [unused]	P0[4]		HiZ Analog Unb
GPIO [unused]	P4[5]		HiZ Analog Unb
GPIO [unused]	P4[2]		HiZ Analog Unb
GPIO [unused]	P4[3]		HiZ Analog Unb
GPIO [unused]	P4[4]		HiZ Analog Unb
GPIO [unused]	P5[1]		HiZ Analog Unb
GPIO [unused]	P5[2]		HiZ Analog Unb
GPIO [unused]	P2[2]		HiZ Analog Unb
GPIO [unused]	P5[0]		HiZ Analog Unb
GPIO [unused]	P1[4]		HiZ Analog Unb
GPIO [unused]	P1[5]		HiZ Analog Unb
GPIO [unused]	P5[3]		HiZ Analog Unb
GPIO [unused]	P1[2]		HiZ Analog Unb
GPIO [unused]	P2[7]		HiZ Analog Unb
GPIO [unused]	P2[4]		HiZ Analog Unb
GPIO [unused]	P2[5]		HiZ Analog Unb
GPIO [unused]	P2[6]		HiZ Analog Unb
GPIO [unused]	P2[3]		HiZ Analog Unb
GPIO [unused]	P6[7]		HiZ Analog Unb
GPIO [unused]	P6[4]		HiZ Analog Unb
GPIO [unused]	P6[5]		HiZ Analog Unb

Name	Port	Type	Reset State
GPIO [unused]	P2[1]		HiZ Analog Unb
GPIO [unused]	P5[6]		HiZ Analog Unb
GPIO [unused]	P15[0]		HiZ Analog Unb
GPIO [unused]	P5[5]		HiZ Analog Unb
GPIO [unused]	P5[7]		HiZ Analog Unb
GPIO [unused]	P6[1]		HiZ Analog Unb
GPIO [unused]	P6[3]		HiZ Analog Unb
GPIO [unused]	P15[4]		HiZ Analog Unb
GPIO [unused]	P2[0]		HiZ Analog Unb
GPIO [unused]	P1[7]		HiZ Analog Unb
GPIO [unused]	P1[6]		HiZ Analog Unb
GPIO [unused]	P15[5]		HiZ Analog Unb
GPIO [unused]	P5[4]		HiZ Analog Unb
P6_2	P6[2]	Dgtl Out	HiZ Analog Unb
RTS	P6[6]	Dgtl Out	HiZ Analog Unb
RX	P0[1]	Dgtl In	HiZ Analog Unb
SIO [unused]	P12[7]		HiZ Analog Unb
SIO [unused]	P12[6]		HiZ Analog Unb
SIO [unused]	P12[5]		HiZ Analog Unb
SIO [unused]	P12[1]		HiZ Analog Unb
SIO [unused]	P12[2]		HiZ Analog Unb
SIO [unused]	P12[0]		HiZ Analog Unb
SIO [unused]	P12[3]		HiZ Analog Unb
SIO [unused]	P12[4]		HiZ Analog Unb
TX	P0[0]	Dgtl Out	HiZ Analog Unb
USB IO [unused]	P15[7]		HiZ Analog Unb
USB IO [unused]	P15[6]		HiZ Analog Unb

Abbreviations used in Table 5 have the following meanings:

- Dgtl In = Digital Input
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the [System Reference Guide](#)
 - o CyPins API routines
- Programming Application Interface section in the [cy_pins component datasheet](#)

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	False
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x80
Stack Size (bytes)	0x0800
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Embedded Trace (ETM)	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

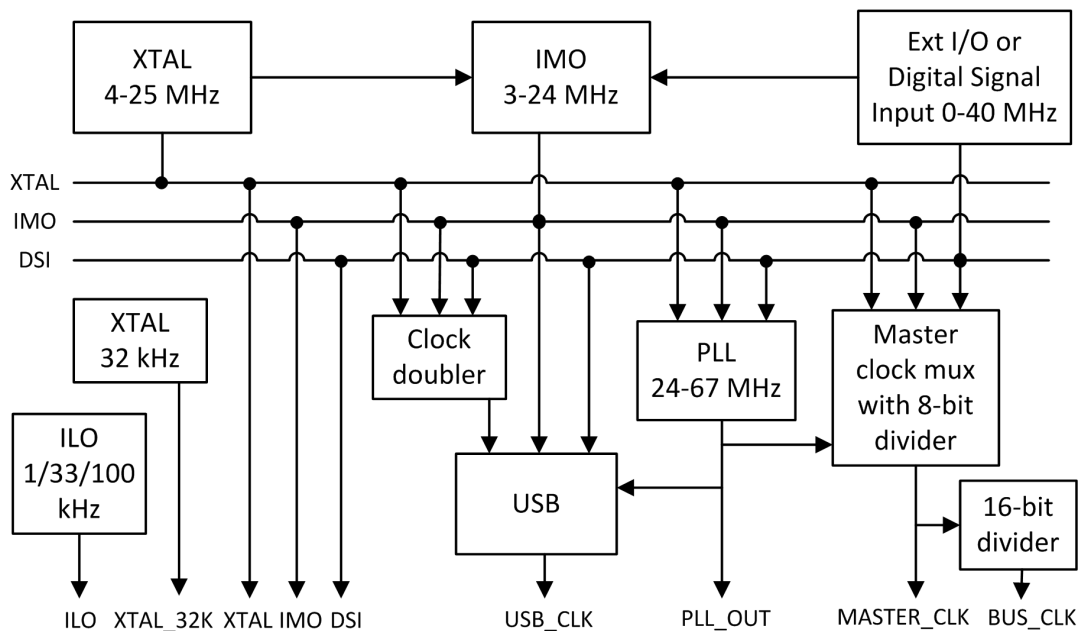
Name	Value
Variable VDDA	False
VDDA (V)	5.5
VDDD (V)	5.5
VDDIO0 (V)	5.5
VDDIO1 (V)	5.5
VDDIO2 (V)	5.5
VDDIO3 (V)	5.5
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
 - o 3 to 74.7 MHz Internal Main Oscillator (IMO) $\pm 1\%$ at 3 MHz
 - o 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
 - o 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
 - o 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
 - o 4 to 25 MHz External Crystal Oscillator (MHzECO)
 - o 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	? MHz	24 MHz	±1	True	True
PLL_OUT	DIGITAL	IMO	24 MHz	24 MHz	±1	True	True
MASTER_CLK	DIGITAL	PLL_OUT	? MHz	24 MHz	±1	True	True
IMO	DIGITAL		3 MHz	3 MHz	±1	True	True
ILO	DIGITAL		? MHz	1 kHz	-50,+100	True	True
USB_CLK	DIGITAL	IMO	48 MHz	? MHz	±0	False	False
XTAL	DIGITAL		25 MHz	? MHz	±0	False	False
XTAL 32kHz	DIGITAL		32.768 kHz	? MHz	±0	False	False
Digital Signal	DIGITAL		? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

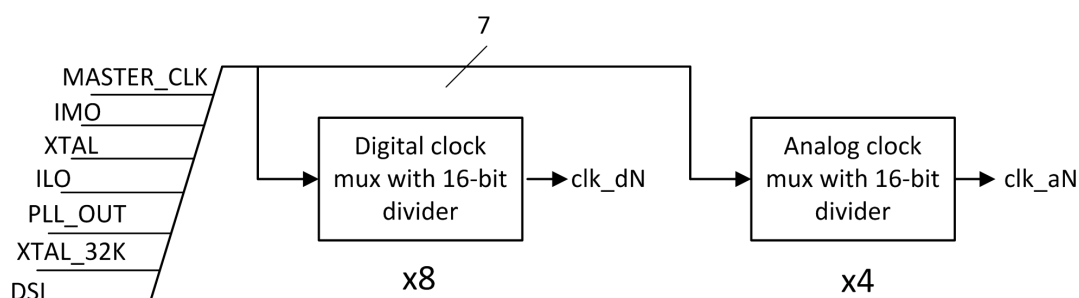


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
Clock_1	DIGITAL	MASTER_CLK	460 kHz	461.538 kHz	±1	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the [PSoC 5 Technical Reference Manual](#)
- Clocking chapter in the [System Reference Guide](#)
 - o CyPLL API routines
 - o CyIMO API routines
 - o CyILO API routines
 - o CyMaster API routines
 - o CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains no interrupt components.

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 5 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 11 lists the Flash protection settings for your design.

Table 11. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x3FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

For more information on Flash memory and protection, please refer to:

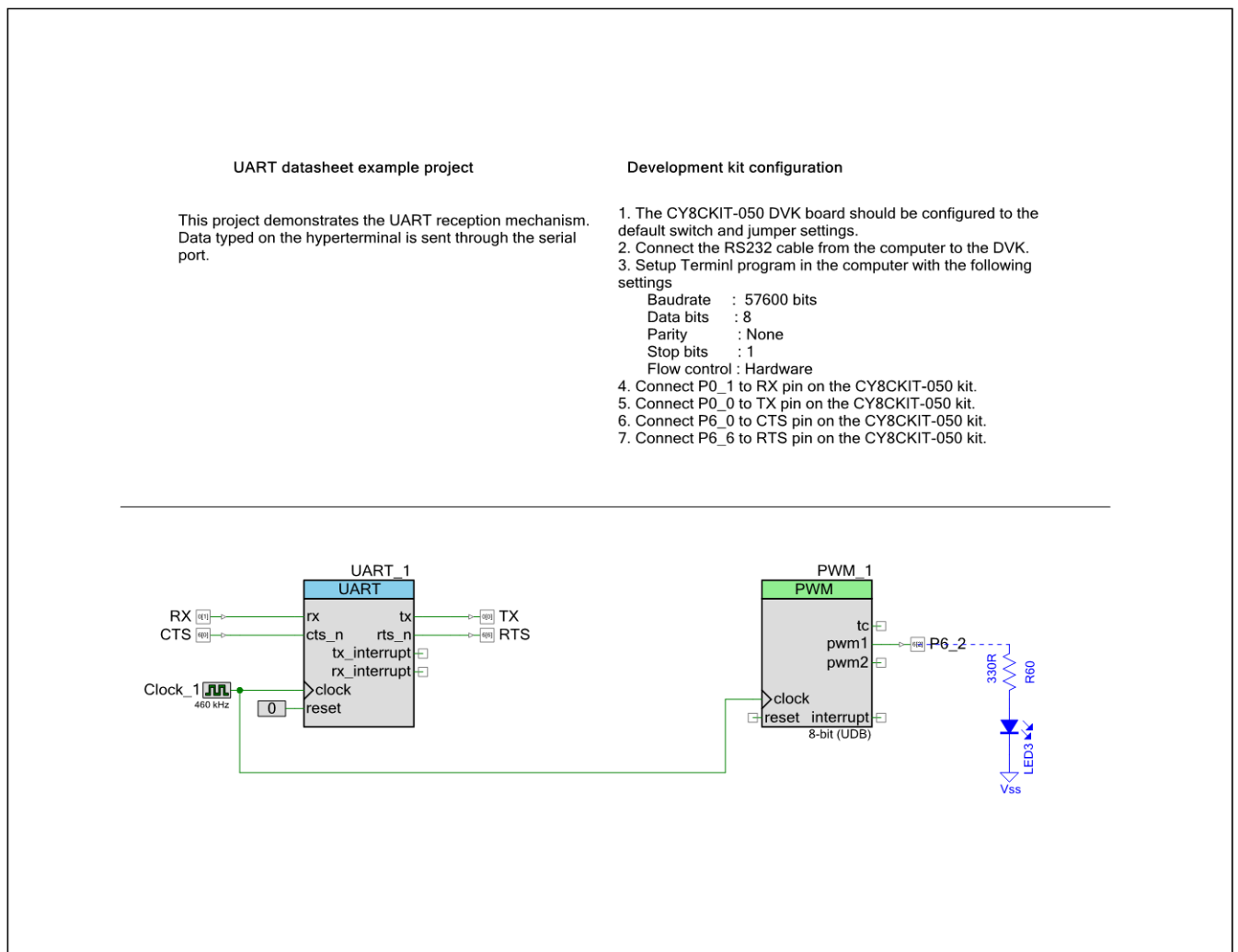
- Flash Protection chapter in the [PSoC 5 Technical Reference Manual](#)
- Flash and EEPROM chapter in the [System Reference Guide](#)
 - o CyWrite API routines
 - o CyFlash API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance [PWM_1](#) (type: PWM_v3_30)
- Instance [UART_1](#) (type: UART_v2_50)

8 Components

8.1 Component type: PWM [v3.30]

8.1.1 Instance PWM_1

Description: 8 or 16-bit Pulse Width Modulator

Instance type: PWM [v3.30]

Datasheet: [online component datasheet for PWM](#)

Table 12. Component Parameters for PWM_1

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture Input. The parameter determines which signal on the capture input is required to capture the current count value to the FIFO.
CompareStatusEdgeSense	true	Enables edge sense detection on compare outputs for use in edge sensitive interrupts
CompareType1	Less	Sets the compare value comparison type setting for the compare 1 output
CompareType2	Less	Sets the compare value comparison type setting for the compare 2 output
CompareValue1	200	Compares Output 1 to value
CompareValue2	62	Compares Output 2 to value
DeadBand	Disabled	Defines whether dead band outputs are desired or not.
DeadTime	1	Defines the number of required dead band clock cycles
DitherOffset	0.00	Allows the user to implement dither to get more bits out of a 8 or 16 bit PWM.
EnableMode	Software Only	Specifies the method of enabling the PWM. This can be either hardware or software.
FixedFunction	false	Determines whether the fixed function counter timer is used or the UDB implementation is used.
InterruptOnCMP1	false	Enables the interrupt on compare1 true event
InterruptOnCMP2	false	Enables the interrupt on compare2 true event
InterruptOnKill	false	Enables the interrupt on a kill event
InterruptOnTC	false	Enables the interrupt on terminal count event
KillMode	Disabled	Parameter to select the kill mode for build time.

Parameter Name	Value	Description
MinimumKillTime	1	Sets the minimum number of clock cycles that a kill must be active on the outputs when KillMode is set to Minimum Kill Time mode
Period	255	Defines the PWM period value
PWMMode	Two Outputs	Defines the overall mode of the PWM
Resolution	8	Defines the bit width of the PWM (8 or 16 bits)
RunMode	Continuous	Defines the run mode options to be either continuous or one shot
TriggerMode	None	Determines the mode of starting the PWM, i.e. triggering the PWM counter to start
UseInterrupt	true	Enables the placement and usage of the status register

8.2 Component type: UART [v2.50]

8.2.1 Instance UART_1

Description: Universal Asynchronous Receiver Transmitter

Instance type: UART [v2.50]

Datasheet: [online component datasheet for UART](#)

Table 13. Component Parameters for UART_1

Parameter Name	Value	Description
Address1	0	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	57600	Sets the target baud rate.
BreakBitsRX	13	Specifies the break signal length for the RX (detection) channel.
BreakBitsTX	13	Specifies the break signal length for the TX channel.
BreakDetect	false	Enables the break detect hardware.
CRCOutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	false	Enables the internal RX interrupt configuration and the ISR.
EnIntTXInterrupt	false	Enables the internal TX interrupt configuration and the ISR.
FlowControl	Hardware	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	false	Enables the external TX enable signal output.
InternalClock	false	Enables the internal clock. This parameter removes the clock input pin.

Parameter Name	Value	Description
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.
InterruptOnTXFifoEmpty	true	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default
IntOnByteRcvd	true	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space
ParityTypeSw	false	This parameter allows the parity type to be changed through software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	4	The size of the RAM space allocated for the RX input buffer.
RXEnable	true	Enables the RX in the UART
TXBitClkGenDP	false	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	4	The size of the RAM space allocated for the TX output buffer.
TXEnable	true	Enables the TX in the UART
Use23Polling	true	Allows the use of 2 out of 3 polling resources on the RX UART sampler.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the [System Reference Guide](#)
 - o Software base types
 - o Hardware register types
 - o Compiler defines
 - o Cypress API return codes
 - o Interrupt types and macros
- Registers
 - o The full PSoC 5 register map is covered in the [PSoC 5 Registers Technical Reference Manual](#)
 - o Register Access chapter in the [System Reference Guide](#)
 - § CY_GET API routines
 - § CY_SET API routines
- System Functions chapter in the [System Reference Guide](#)
 - o General API routines
 - o CyDelay API routines
 - o CyVd Voltage Detect API routines
- Power Management
 - o Power Supply and Monitoring chapter in the [PSoC 5 Technical Reference Manual](#)
 - o Low Power Modes chapter in the [PSoC 5 Technical Reference Manual](#)
 - o Power Management chapter in the [System Reference Guide](#)
 - § CyPm API routines
- Watchdog Timer chapter in the [System Reference Guide](#)
 - o CyWdt API routines
- Cache Management
 - o Cache Controller chapter in the [PSoC 5 Technical Reference Manual](#)
 - o Cache chapter in the [System Reference Guide](#)
 - § CyFlushCache() API routine